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Attorney Docket No.: 42P12718

Amendments to the Claims

Claim 1. (currently amended) A method of sampling data, comprising:  
gathering a first data sample during execution of a program on a computing device;  
executing the program during a random inter-sample period; and  
gathering a second data sample following the inter-sample period, wherein the first and second data samples include a level of memory utilization during program execution, and wherein the first and second data samples form at least a portion of a set of data samples, the set of data samples to be used to determine a measure of performance of the computing device while executing the program.

Claim 2. (original) The method of claim 1, wherein executing the program comprises:  
generating an inter-sample count; and  
decrementing the inter-sample count to zero before gathering the second data sample.

Claim 3. (original) The method of claim 2, further comprising:  
performing overhead operations during the inter-sample period.

Claim 4. (original) The method of claim 3, wherein the inter-sample count is longer than an execution time required to perform the overhead operations.

Claim 5. (original) The method of claim 3, wherein the overhead operations include at least one of decrementing the inter-sample count, storing a data sample, and performing a calculation based on a data sample.

Claim 6. (currently amended) The method of claim 1, wherein gathering the first data sample comprises:  
resetting data gathering hardware,  
executing the program during a sampling period; and

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stopping the data gathering hardware at the end of the sampling period, wherein data samples in the set of data samples are statistically distributed.

Claim 7. (original) The method of claim 1, wherein gathering the first data sample comprises:

starting data gathering hardware,  
executing the program during a sampling period; and  
stopping the data gathering hardware at the end of the sampling period.

Claim 8. (original) The method of claim 7, wherein the data gathering hardware comprises at least one event counter register.

Claim 9. (original) The method of claim 2, wherein generating the inter-sample count comprises:

enabling a linear feedback shift register to produce a bit pattern.

Claim 10. (original) The method of claim 9, wherein the linear feedback shift register is configured to produce a bit pattern that corresponds to a primitive trinomial.

Claim 11. (currently amended) An article comprising a machine-readable medium that stores machine-executable instructions for sampling data, the instructions causing a machine to:

gather a first data sample during execution of a program on the machine;  
execute a program during a random inter-sample period; and  
gather a second data sample following the inter-sample period, wherein the first and second data samples include a level of memory utilization during program execution, and wherein the first and second data samples form at least a portion of a set of data samples, the set of data samples to be used to determine a measure of performance of the computing device while executing the program.

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Claim 12. (original) The article of claim 11, wherein instructions causing a machine to execute the program comprises instructions causing a machine to:

generate an inter-sample count; and  
decrement the inter-sample count to zero before gathering the second data sample.

Claim 13. (original) The article of claim 12, comprising instructions causing the machine to:

perform overhead operations during the inter-sample period.

Claim 14. (original) The article of claim 13, wherein instructions causing a machine to generate an inter-sample count comprise instructions causing a machine to:

generate an inter-sample count longer than an execution time required to perform the overhead operations.

Claim 15. (original) The article of claim 13, wherein instructions causing a machine to perform overhead operations include instructions to cause a machine to perform at least one of decrement the inter-sample count, store the data sample, and perform a calculation based on a data sample.

Claim 16. (currently amended) The article of claim 11, wherein instructions causing a machine to gather a first data sample comprise instructions to cause a machine to:

start data gathering hardware;  
gather the first data sample during execution the program; and  
stop the data gathering hardware, wherein data samples in the set of data samples are statistically distributed.

Claim 17. (original) The article of claim 16, wherein the data gathering hardware comprises at least one event counter register.

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Claim 18. (original) The article of claim 12, wherein instructions causing a computer to generate an inter-sample count comprises instructions causing a machine to:

enable a linear feedback shift register to produce a bit pattern.

Claim 19. (original) The article of claim 18, wherein the linear feedback shift register is configured to produce a bit pattern that corresponds to a primitive trinomial.

Claim 20. (currently amended) An apparatus for sampling data, comprising:  
a memory that stores executable instructions; and  
a computer processor that executes the instructions to:

gather a first data sample during execution of an application on the computer processor;

execute the application during a statistically distributed random inter-sample period; and

gather a second data sample following an the inter-sample period, wherein the first and second data samples include a level of memory utilization during application execution, and wherein the first and second data samples form at least a portion of a set of data samples, the set of data samples to be used to determine a measure of performance of the computer processor while executing the application.

Claim 21. (original) The apparatus of claim 20, wherein the computer processor further comprises:

a decrementing register, wherein the computer processor executes instructions to:

generate an inter-sample count,

store the inter-sample count in the decrementing register, and

decrement the inter-sample count to zero before gathering the second data sample.

Claim 22. (previously presented) The apparatus of claim 21, wherein the computer processor executes instructions to:

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perform overhead operations during the inter-sample period, and wherein the application is running during the inter-sample period.

Claim 23. (original) The apparatus of claim 22, wherein the computer processor executes instructions to:

generate an inter-sample count that is longer than an execution time required to perform the overhead operations.

Claim 24. (original) The apparatus of claim 22, wherein the computer processor executes instructions to:

perform overhead operations that include instructions for at least one of decrementing the inter-sample count, storing a data sample, and perform a calculation based on a data sample.

Claim 25. (currently amended) The apparatus of claim 20, wherein the computer processor comprises:

data gathering hardware, and wherein the computer processor executes instructions to:  
start the data gathering hardware, wherein starting the data gathering hardware ~~after the inter-sample period~~ is to end the inter-sample period; and  
stop the data gathering hardware to commence the inter-sample period.

Claim 26. (original) The apparatus of claim 25, wherein the data gathering hardware comprises at least one event counter register.

Claim 27. (original) The apparatus of claim 21, wherein the computer processor comprises:

a linear feedback shift register, and wherein the computer processor executes an instruction to enable the linear feedback shift register to produce a bit pattern that corresponds the inter-sample count.

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Claim 28. (original) The apparatus of claim 27, wherein the linear feedback shift register is configured to produce a bit pattern that corresponds to a primitive trinomial.